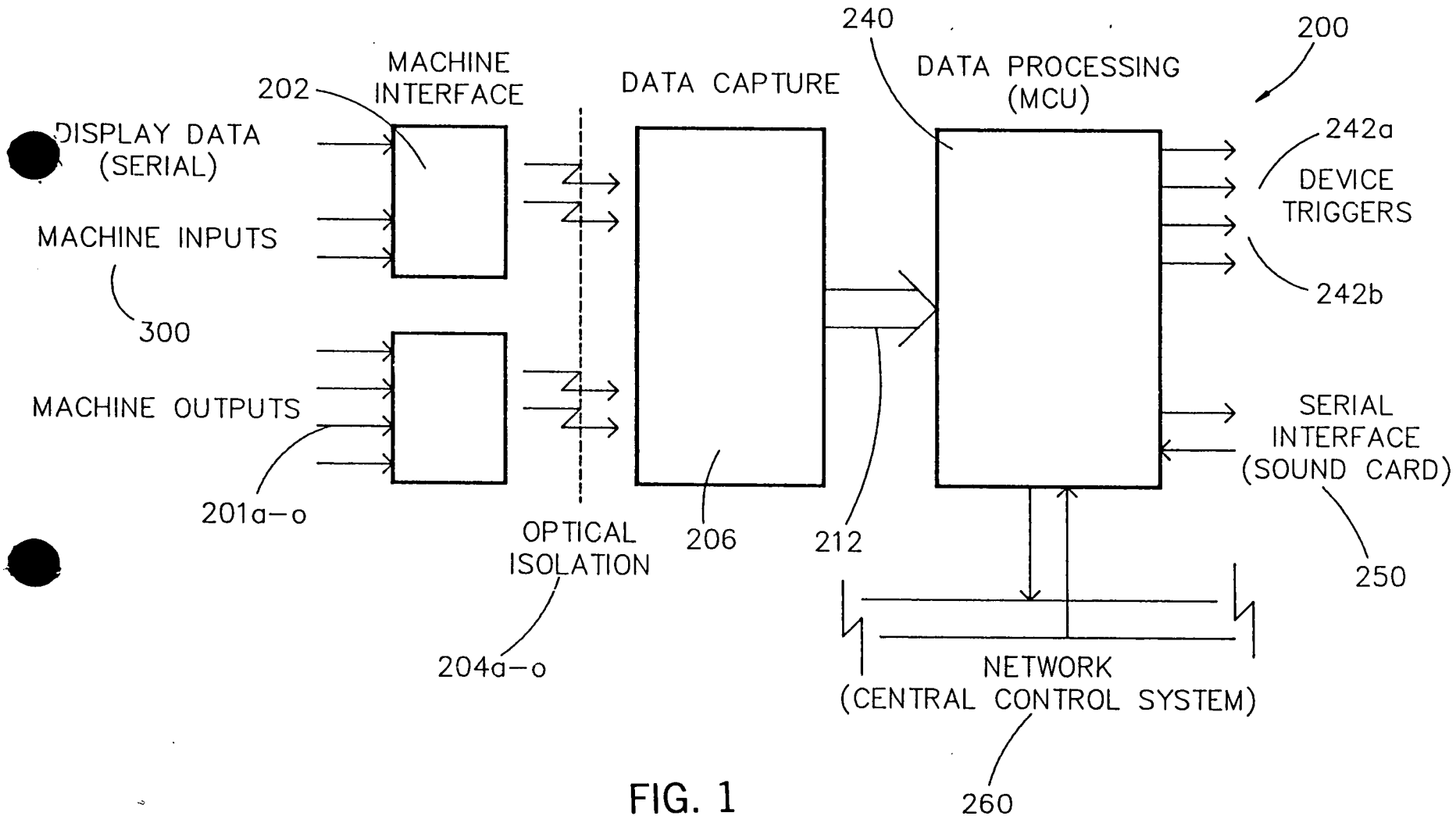
240
200
MACHINE
INTERFACE
202
DATA CAPTURE
DATA PROCESSING
(MCU)
DISPLAY DATA
(SERIAL)
242a
DEVICE
TRIGGERS
MACHINE INPUTS
242b
300
MACHINE OUTPUTS
SERIAL
INTERFACE
(SOUND CARD)
201a–o
OPTICAL
ISOLATION
206
212
250
204a–o
NETWORK
(CENTRAL CONTROL SYSTEM)
260

FIG. 1

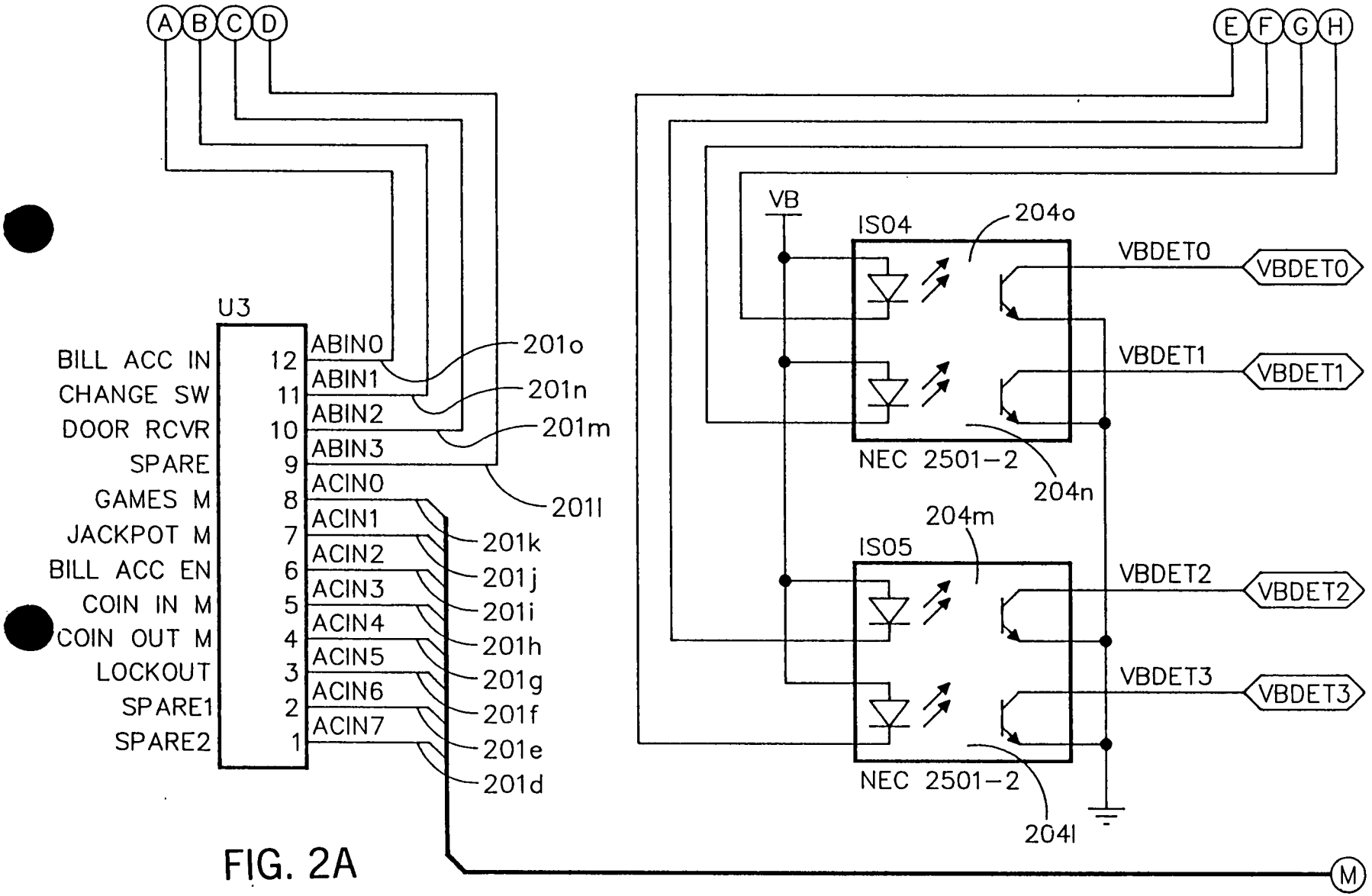
A
B
C
D
E
F
G
H
U3
BILL ACC IN 12
CHANGE SW 11
DOOR RCVR 10
SPARE 9
GAMES M 8
JACKPOT M 7
BILL ACC EN 6
COIN IN M 5
COIN OUT M 4
LOCKOUT 3
SPARE1 2
SPARE2 1
ABIN0
ABIN1
ABIN2
ABIN3
ACIN0
ACIN1
ACIN2
ACIN3
ACIN4
ACIN5
ACIN6
ACIN7
201o
201n
201m
201l
201k
201j
201i
201h
201g
201f
201e
201d
VB
IS04
204o
VBDET0
VBDET1
NEC 2501-2
204n
204m
IS05
VBDET2
VBDET3
NEC 2501-2
204l
M

FIG. 2A

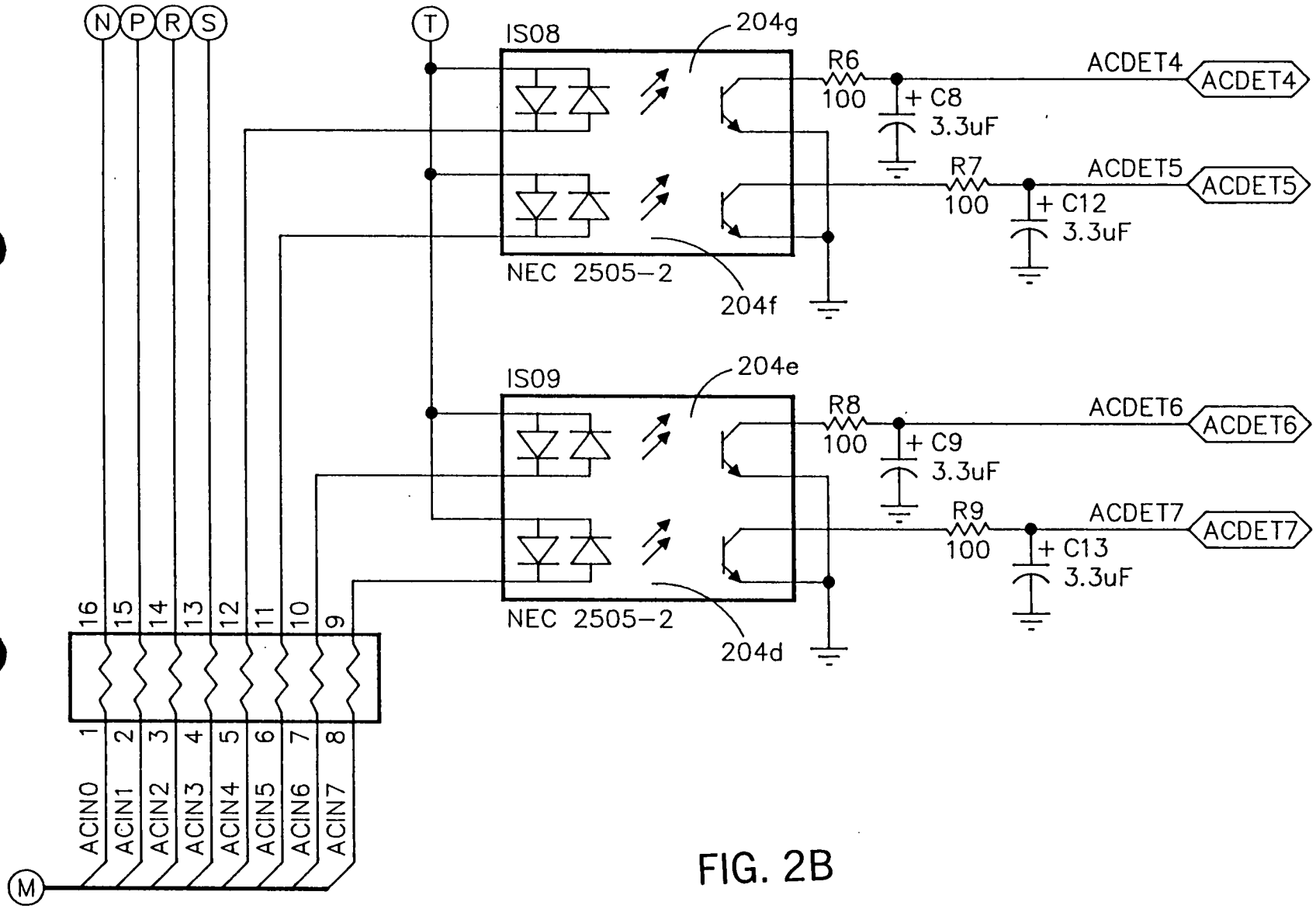
N
P
R
S
T
M
IS08
204g
NEC 2505-2
204f
IS09
204e
NEC 2505-2
204d
R6
100
+ C8
3.3uF
R7
100
+ C12
3.3uF
R8
100
+ C9
3.3uF
R9
100
+ C13
3.3uF
ACDET4
ACDET4
ACDET5
ACDET5
ACDET6
ACDET6
ACDET7
ACDET7
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
ACIN0
ACIN1
ACIN2
ACIN3
ACIN4
ACIN5
ACIN6
ACIN7

FIG. 2B

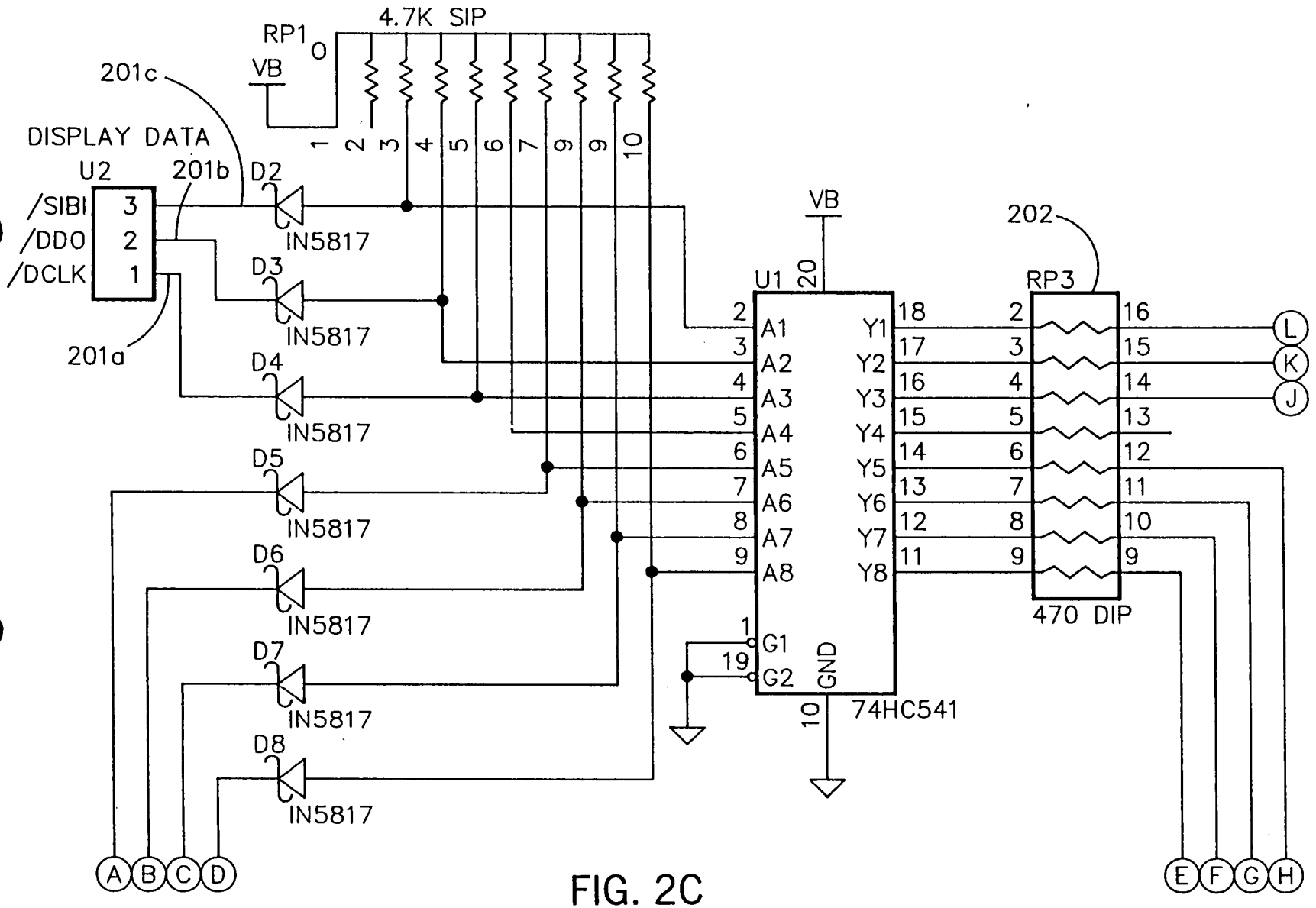
4.7K SIP
RP1
VB
201c
DISPLAY DATA
U2
201b
/SIBI
/DDO
/DCLK
201a
D2
D3
D4
D5
D6
D7
D8
IN5817
VB
U1
74HC541
GND
G1
G2
202
RP3
470 DIP
A
B
C
D
E
F
G
H
L
K
J

FIG. 2C

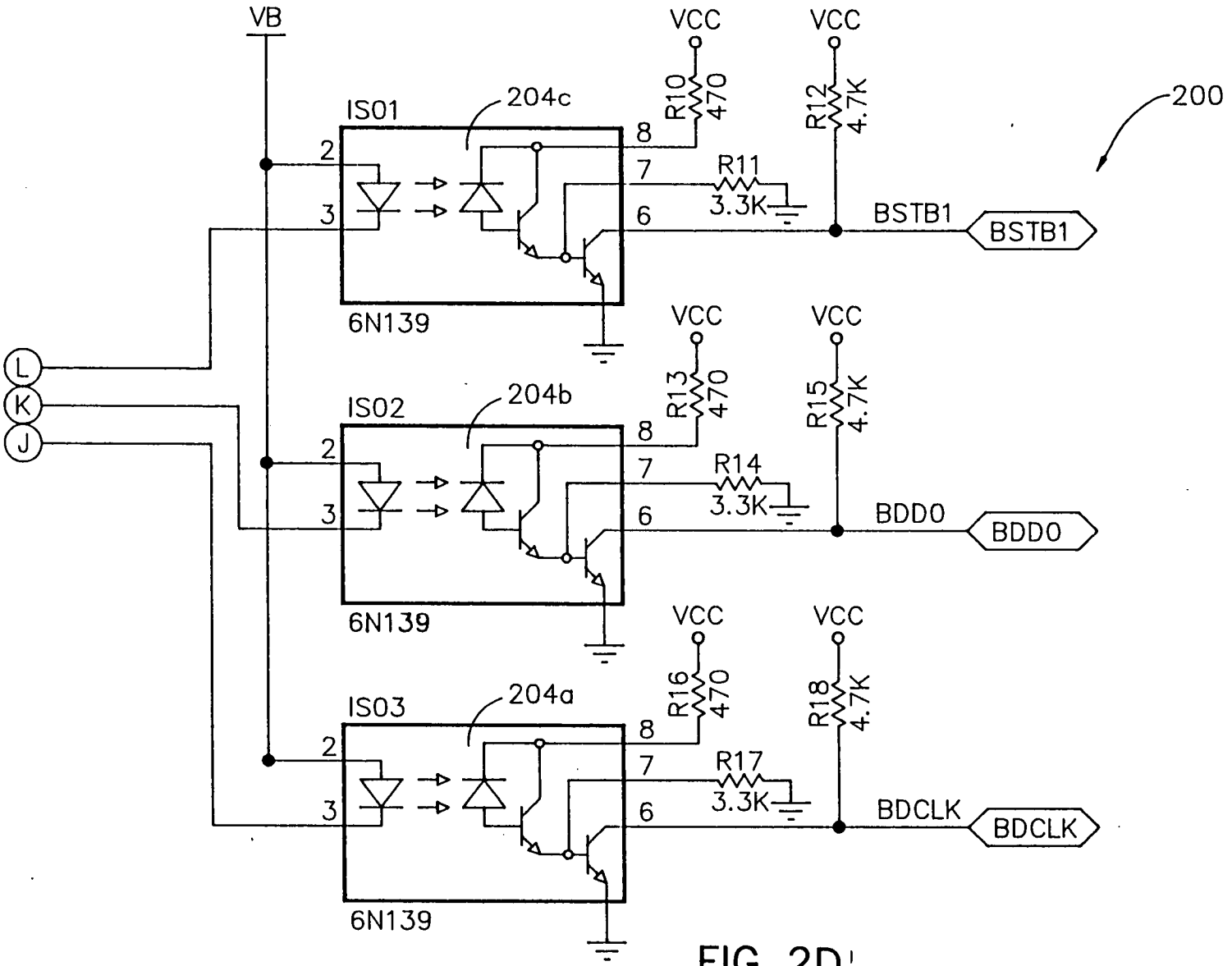
VB
VCC
VCC
200
IS01
204c
R10
470
R12
4.7K
2
3
8
7
6
R11
3.3K
BSTB1
BSTB1
6N139
L
K
J
IS02
204b
R13
470
R15
4.7K
R14
3.3K
BDD0
BDD0
6N139
IS03
204a
R16
470
R18
4.7K
R17
3.3K
BDCLK
BDCLK
6N139

FIG. 2D'

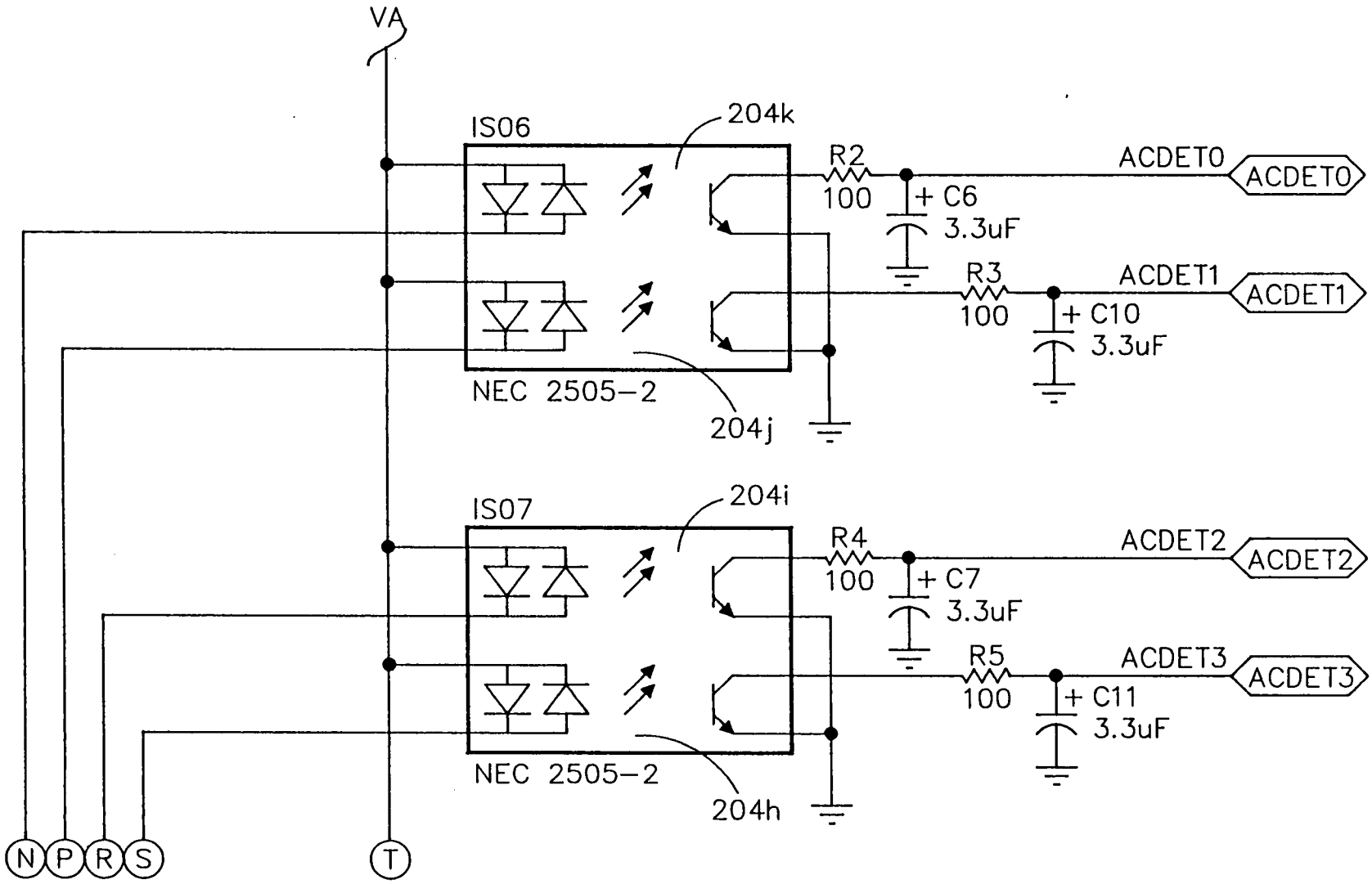
VA
IS06
204k
R2
100
+ C6
3.3uF
ACDET0
ACDET0
R3
100
+ C10
3.3uF
ACDET1
ACDET1
NEC 2505-2
204j
IS07
204i
R4
100
+ C7
3.3uF
ACDET2
ACDET2
R5
100
+ C11
3.3uF
ACDET3
ACDET3
NEC 2505-2
204h
N
P
R
S
T

FIG. 2E

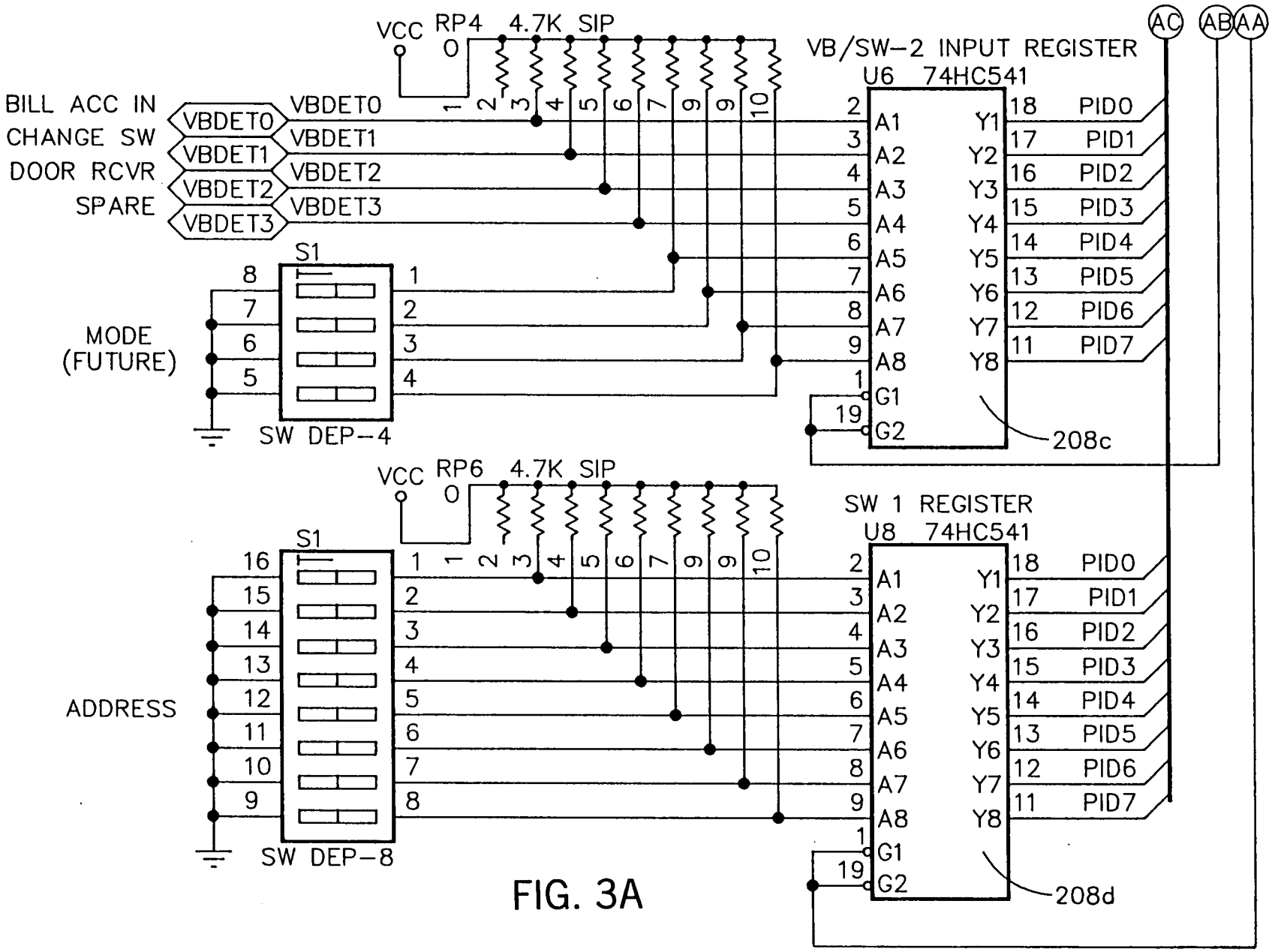
VCC RP4 4.7K SIP
VB/SW-2 INPUT REGISTER
U6 74HC541
BILL ACC IN
CHANGE SW
DOOR RCVR
SPARE
VBDET0
VBDET1
VBDET2
VBDET3
S1
MODE
(FUTURE)
SW DEP-4
208c
VCC RP6 4.7K SIP
SW 1 REGISTER
U8 74HC541
ADDRESS
SW DEP-8
208d
AC
AB
AA
PID0
PID1
PID2
PID3
PID4
PID5
PID6
PID7
A1
A2
A3
A4
A5
A6
A7
A8
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
G1
G2

FIG. 3A

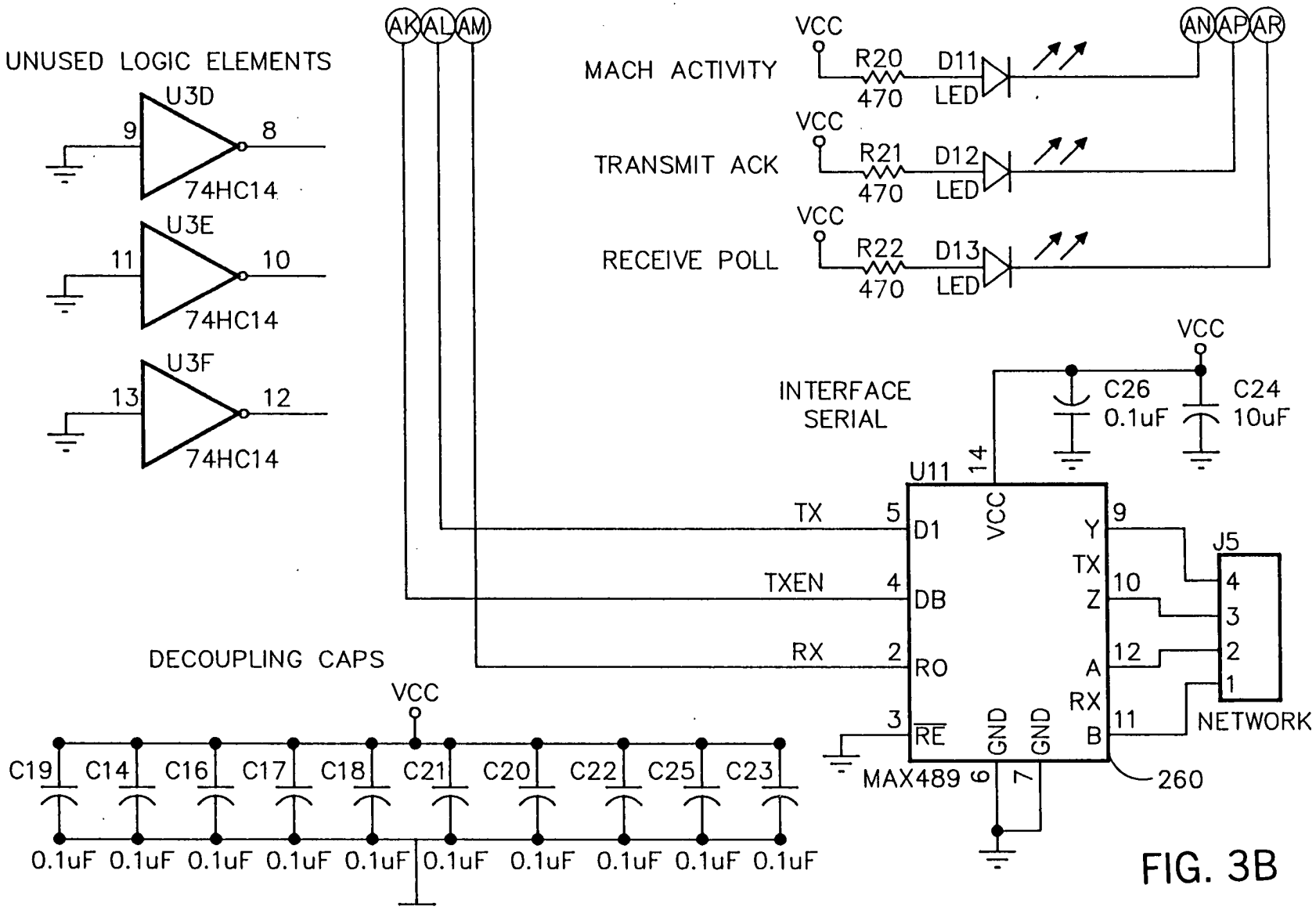
UNUSED LOGIC ELEMENTS
U3D
9
8
74HC14
U3E
11
10
74HC14
U3F
13
12
74HC14
AK
AL
AM
MACH ACTIVITY
TRANSMIT ACK
RECEIVE POLL
VCC
R20
470
D11
LED
R21
D12
R22
D13
AN
AP
AR
INTERFACE
SERIAL
C26
0.1uF
C24
10uF
U11
14
TX
5
D1
TXEN
4
DB
RX
2
RO
3
RE
GND
7
9
Y
TX
10
Z
12
A
RX
11
B
J5
NETWORK
MAX489
6
260
DECOUPLING CAPS
C19
C14
C16
C17
C18
C21
C20
C22
C25
C23
0.1uF

FIG. 3B

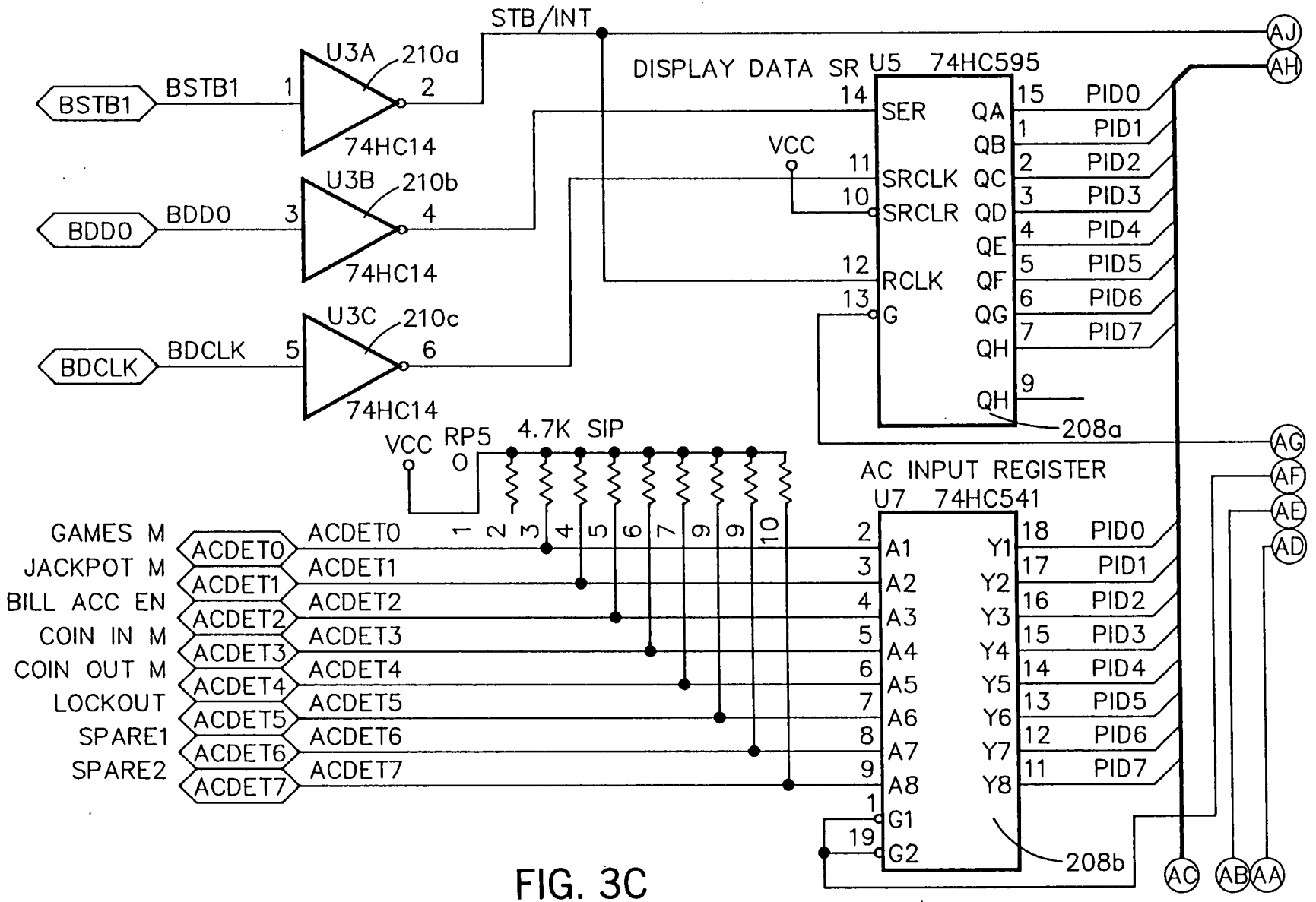
STB/INT
U3A
210a
BSTB1
BSTB1
1
2
74HC14
U3B
210b
BDD0
BDD0
3
4
74HC14
U3C
210c
BDCLK
BDCLK
5
6
74HC14
DISPLAY DATA SR U5 74HC595
14
SER
QA
15
PID0
QB
1
PID1
VCC
11
SRCLK
QC
2
PID2
10
SRCLR
QD
3
PID3
QE
4
PID4
12
RCLK
QF
5
PID5
13
G
QG
6
PID6
QH
7
PID7
9
QH
208a
VCC
RP5
4.7K SIP
0
1
2
3
4
5
6
7
9
9
10
AC INPUT REGISTER
U7 74HC541
GAMES M
JACKPOT M
BILL ACC EN
COIN IN M
COIN OUT M
LOCKOUT
SPARE1
SPARE2
ACDET0
ACDET1
ACDET2
ACDET3
ACDET4
ACDET5
ACDET6
ACDET7
2
A1
Y1
18
PID0
3
A2
Y2
17
PID1
4
A3
Y3
16
PID2
5
A4
Y4
15
PID3
6
A5
Y5
14
PID4
7
A6
Y6
13
PID5
8
A7
Y7
12
PID6
9
A8
Y8
11
PID7
1
G1
19
G2
208b
AJ
AH
AG
AF
AE
AD
AC
AB
AA

FIG. 3C

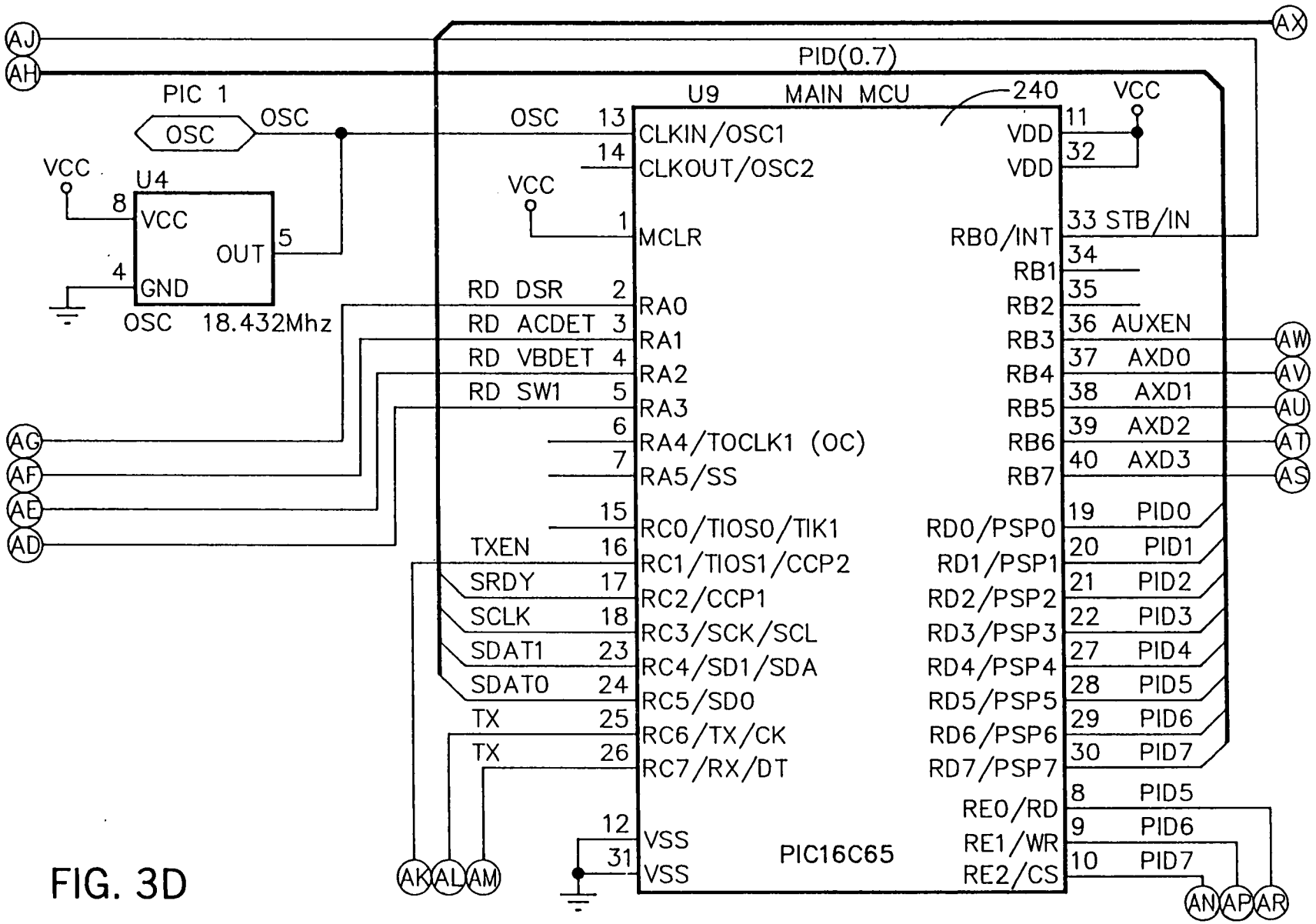
AJ
AH
AX
PID(0.7)
PIC 1
OSC
OSC
U9
MAIN MCU
240
VCC
VCC
U4
8
VCC
OUT
5
4
GND
OSC 18.432Mhz
OSC 13
CLKIN/OSC1
14
CLKOUT/OSC2
VCC
1
MCLR
RD DSR 2
RA0
RD ACDET 3
RA1
RD VBDET 4
RA2
RD SW1 5
RA3
6
RA4/TOCLK1 (OC)
7
RA5/SS
15
RC0/TIOS0/TIK1
TXEN 16
RC1/TIOS1/CCP2
SRDY 17
RC2/CCP1
SCLK 18
RC3/SCK/SCL
SDAT1 23
RC4/SD1/SDA
SDAT0 24
RC5/SD0
TX 25
RC6/TX/CK
TX 26
RC7/RX/DT
12
VSS
31
VSS
PIC16C65
VDD 11
VDD 32
RB0/INT 33 STB/IN
RB1 34
RB2 35
RB3 36 AUXEN
RB4 37 AXD0
RB5 38 AXD1
RB6 39 AXD2
RB7 40 AXD3
RD0/PSP0 19 PID0
RD1/PSP1 20 PID1
RD2/PSP2 21 PID2
RD3/PSP3 22 PID3
RD4/PSP4 27 PID4
RD5/PSP5 28 PID5
RD6/PSP6 29 PID6
RD7/PSP7 30 PID7
RE0/RD 8 PID5
RE1/WR 9 PID6
RE2/CS 10 PID7
AG
AF
AE
AD
AK
AL
AM
AW
AV
AU
AT
AS
AN
AP
AR

FIG. 3D

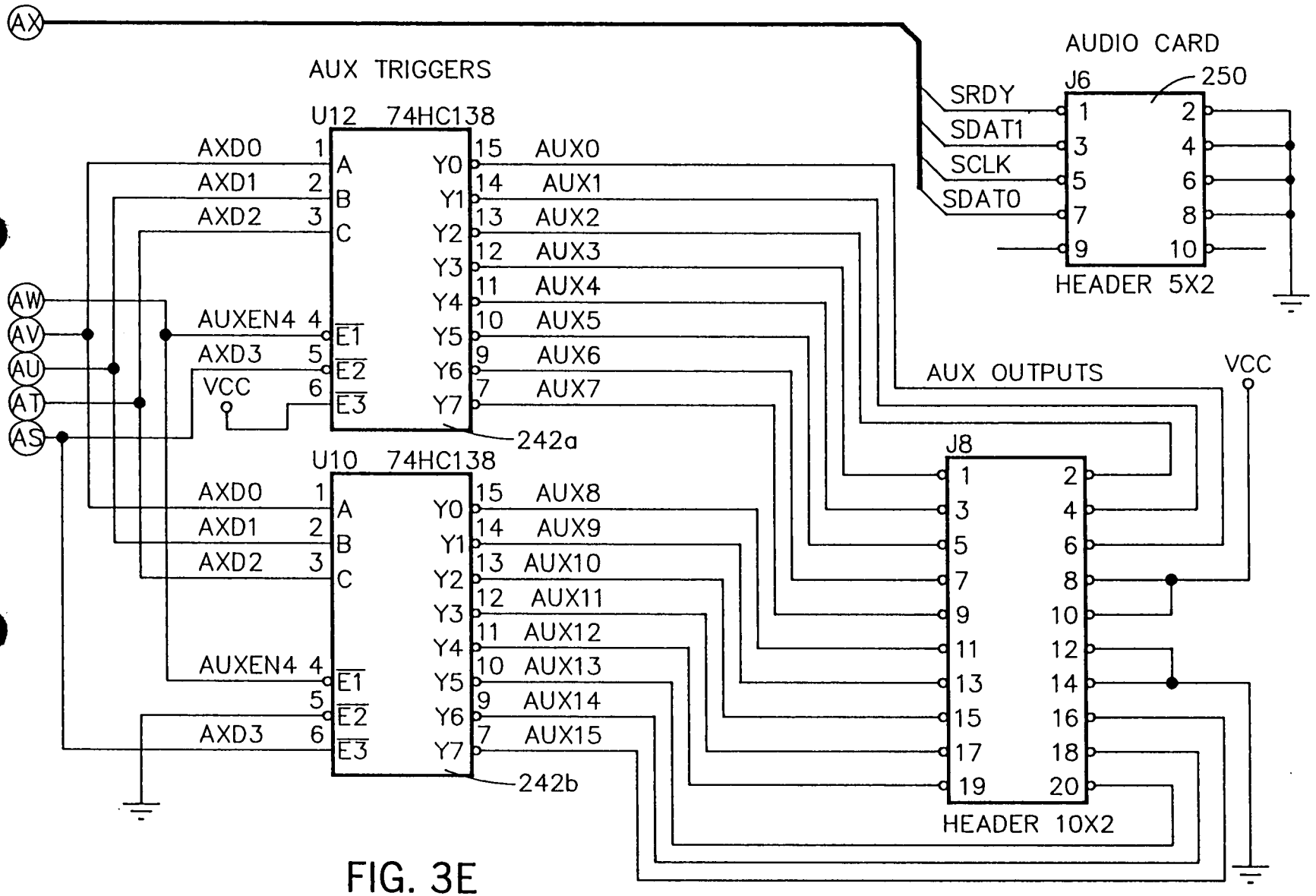
AX
AUDIO CARD
AUX TRIGGERS
U12 74HC138
AXD0 1
AXD1 2
AXD2 3
AUXEN4 4
AXD3 5
VCC 6
A
B
C
E1
E2
E3
Y0 15 AUX0
Y1 14 AUX1
Y2 13 AUX2
Y3 12 AUX3
Y4 11 AUX4
Y5 10 AUX5
Y6 9 AUX6
Y7 7 AUX7
242a
U10 74HC138
AXD0 1
AXD1 2
AXD2 3
AUXEN4 4
5
AXD3 6
Y0 15 AUX8
Y1 14 AUX9
Y2 13 AUX10
Y3 12 AUX11
Y4 11 AUX12
Y5 10 AUX13
Y6 9 AUX14
Y7 7 AUX15
242b
AW
AV
AU
AT
AS
SRDY
SDAT1
SCLK
SDAT0
J6
250
1 2
3 4
5 6
7 8
9 10
HEADER 5X2
AUX OUTPUTS
VCC
J8
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
HEADER 10X2

FIG. 3E